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Analysis and Design of Interleaved DCM Buck-Boost Derived Three-Phase PFC Converter for MEA

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***Abstract*—In more electric aircrafts (MEAs), the synchronous generators are connected directly to the turbo-engine to develop a constant voltage variable frequency (CVVF) AC supply bus. In addition, the MEA has adopted high voltage DC bus in its power system to cater the various categories of load used by aircraft. Therefore, this change in power paradigm has created a requirement for AC-DC power factor correction (PFC) converters to convert CVVF AC to constant DC with high power quality in a reliable manner. In this paper, a three-phase interleaved buck-boost-derived PFC converter operated in discontinuous current conduction mode to realize the inherent unity power factor (UPF) operation for MEA wide range of supply frequency. The benefits of the proposed converter are higher power density, efficiency, and reliability. The advantages of the proposed converter are demonstrated by performing an analytical comparison with the single-cell three-phase buck-boost derived PFC converter and presented the relevant results. The experimental results from a 2.0 kW laboratory concept-proof hardware prototype have been provided to confirm the proposed converter UPF operation for wide range supply frequencies. A low input power factor of 0.9996 and a minimum current THD of 2.52 % are recorded from the developed prototype.**

***Keywords—Power factor correction, more electric aircraft, interleaved, buck-boost-derived, AC-DC converter*.**

I. INTRODUCTION

The global earth temperatures are raising rapidly due to the increased concentration of greenhouse gases in air. The sources for greenhouse gas emissions include transportation, industries, thermal plants, burning of wood and fossil fuels, etc. In the total manmade emissions, the total transportation alone accounts for 12%, and among that the aviation accounts for 3% and is expected to increase further by 3% in coming twenty years [1]. Therefore, to reduce the aviation impact on global climatic change, the advisory council for aeronautics research in Europe (ACARE) has set the goals for 2020 and 2050 to be met by a single empty aircraft [2], [3], as listed in Table I. The goals for 2020 include 50% reduction in carbon emissions, 80% reduction in NOx emissions, and 50% reduction in fuel consumption. In view of achieving these goals, the conventional aircrafts are moving towards more electric by replacing the existing conventional bulky hydraulic, pneumatic, and mechanical subsystems with the compact more efficient electrical systems [4], [5]. During this movement, a heavy mechanical constant speed gearbox sits between the turbo engine and the synchronous generator has been removed which resulted in a variable frequency 300 to 800 Hz AC supply bus in more electric aircraft (MEA) power system [4]- [9]. In addition, the MEA power system has adopted a high voltage 270 V DC bus to cater the various categories of load used by aircraft, and to further reduce the size and weight of the cables. Moreover, the conventional centralized hydraulic pumps are eliminated and replaced with localized electro hydrostatic actuators (EHA) which are driven by the electric motors [10]. So, the EHA interface to the MEA AC grid requires rectifier system with power ranging typically from 5 kW to 10 kW [11]. These rectifiers are driven with the requirements of high-power quality, reliability, power density, and efficiency. Further, the rectifiers should provide degraded power operation in case of a phase open fault.

TABLE I
ACARE GOALS FOR 2020 AND 2050

Goals	2020	2050
CO_2 emissions reduction	50 %	75 %
NO_X emissions reduction	80 %	90 %
External noise reduction	50 %	65 %
Fuel consumption reduction	50 %	-----

In MEAs, the traditional passive diode-based auto-transformer rectifier units are being replaced with the active-switching rectifier units to improve the power density and power quality of the electrical system [12]. The active rectifiers comprise power factor correction (PFC) unit at their front end to obtain high input power quality and regulated DC output voltage. In [13]-[17], a detailed review of the three-phase active PFC rectifiers has been presented. Alike other power converters, the active PFC rectifiers can be operated either in continuous current conduction mode (CCM) or discontinuous current conduction mode (DCM) which is basically discriminated by the inductor current continuity in the converter. The CCM PFC control is a two-loop cascaded control with outer voltage control loop for regulating the output voltage, and with inner current control loop for shaping the input current sinusoidal and for maintaining the unity power factor (UPF) operation [18]-[22]. Further, it requires phase-locked-loop (PLL) and higher bandwidth inner current controllers. The variable supply frequency operation of MEA complicates both the PLL and the inner current controller designs. Moreover, this control needs at least five sensors for implementing the PFC control. In contrast, the DCM operation inherently achieves PFC and eliminates the need for inner current control loop. In DCM, in every switching cycle, the current drawn from input source is directly proportional to the input voltage at that instant. It means that the average input current inherently follows the input voltage both in phase and shape and exhibits an inherent UPF operation [23]-[25]. Therefore, the DCM operation eliminates the inner current shaping loop and needs only the voltage control loop which in turn needs only single sensor. The reduction in sensors count adds several benefits such as low cost, higher reliability, higher frequency noise robustness, higher power density, and a slight improvement in system efficiency [26]. Therefore, considering the certain

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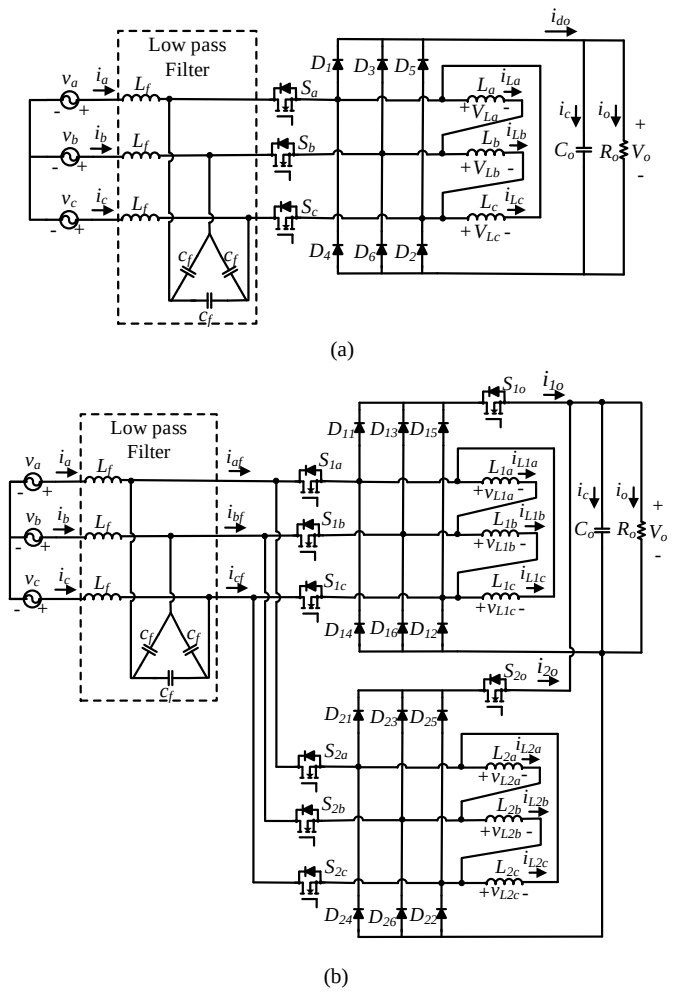

(a)

(b)

Fig. 1. (a) Three-phase buck-boost-derived PFC converter [32]; (b) proposed three-phase interleaved buck-boost-derived PFC converter.

limitations of the CCM operation, and the benefits of DCM operation for variable supply frequency, the DCM operation is considered in this paper.

However, the DCM operation bounds the converter operating range due to its low inductance causes high current peaks through switches and diodes, which consequently necessitates high current rated semiconductor components, and large size filters. But these limitations can be overcome by adopting interleaved technique [27]-[29]. The interleaving of converters is a popular approach in power electronics where two or more identical converter cells are connected in parallel at both input and output which allows the sharing of total power equally among the converter cells. Thus, the power processed by each converter cell will be reduced, which further reduces the current peaks through the semiconductor components. The merits of the interleaved technique are the reduced filter current ripples, reduced filter size, higher power density, higher reliability, and improved efficiency. Further, the interleaving of converters will elevate the overall power level of the rectifier system by sharing the total power among the interleaved cells [31].

In [32], a three-phase buck-boost-derived PFC converter for MEA operated in DCM is presented. The merits of this converter are reduced number of components, simplified control, and high efficiency in its category. Therefore, considering the merits of the interleaved technique and the three-phase buck-boost-derived

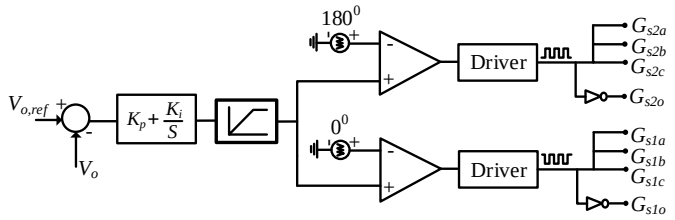

Fig. 2. The control scheme for the proposed converter.

PFC converter, an interleaved version of the three-phase buck-boost-derived PFC converter is presented and analyzed in this paper. The main contributions of the paper are as follow

1) The proposal of the modified version of the converter [32] with an added switch to provide the bidirectional blocking capability and to evade the circulating current for the interleaved operation.
2) Zero switching loss operation of the extra switch as it is operated with zero voltage switching during turn on and zero current switching during turn off.
3) Comparison of the proposed interleaved converter with the single cell converter [32] in terms of power density, efficiency, and reliability.
4) Validation of the proposed interleaved converter operation and control with experimental results from a 2.0 kW laboratory prototype.
5) Comparison of the proposed converter with the sate-of-the-art interleaved boost converters.

The proposed interleaved three-phase buck-boost-derived PFC converter is presented and analyzed in section II. The converter design is presented in section III. The analytical results for evidencing the merits of the proposed interleaved converter is presented in section IV by comparing it with the single-cell converter for the same operating conditions. The experimental results from a 2.0 kW concept-proof laboratory prototype to demonstrate the converter UPF operation is presented in section V. The paper conclusions are provided in section VI.

II. Proposed Converter and Steady-State Analysis

A. Proposed Converter

Fig. 1(a) shows the three-phase buck-boost-derived PFC converter [32] with three unidirectional blocking switches with one in each phase. The three switches are operated synchronously with the same gate signal. This converter cannot be used in this form for interleaved operation due to its merely unidirectional blocking capability at the input creates circulating currents between the two converter cells for the duty cycle $d > 0.5$ which further aggravates the converter losses and degrades the PFC performance. Therefore, to provide the bidirectional blocking capability, one extra switch is placed at output of the bridge rectifier and this switch is operated in complementary to the synchronous input switches for the entire range of duty operation. Fig. 1(b) shows the proposed three-phase interleaved buck-boost-derived PFC converter with two modified cells of Fig. 1(a) which are connected in parallel at both the input and the output. Each cell of the converter is designed for DCM operation to realize the natural PFC at variable frequency AC mains. The DCM operation ensures the zero current turn on for the input switches and zero current turn off for the added output switches. The added output switches also turn on with zero voltage switching due to the forward biasing of the antiparallel

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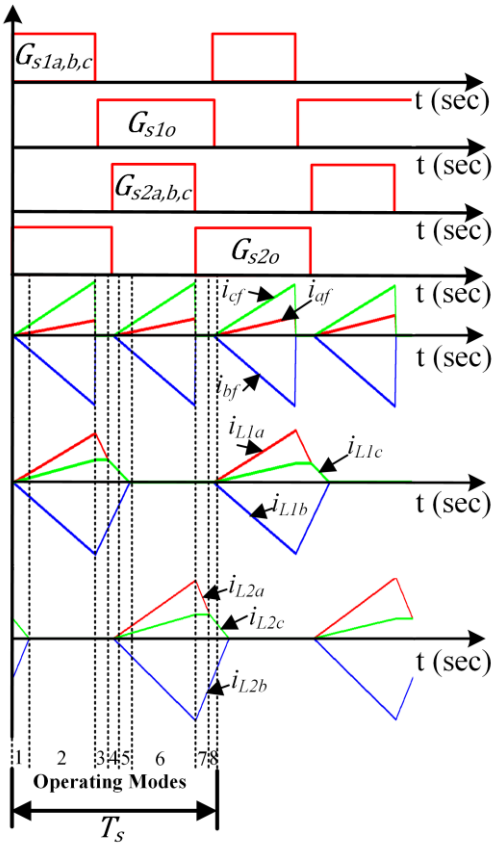

Fig. 3. The converter current waveforms for duty cycle $d \leq 0.5$.

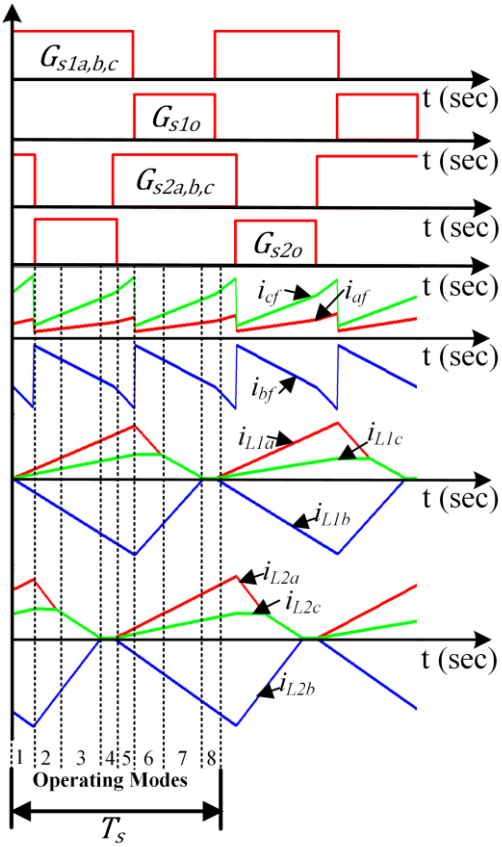

Fig. 4. The converter current waveforms for duty cycle $d > 0.5$.

diode by the output voltage. Therefore, the switching losses of the added output switches are zero theoretically.

Fig. 2 shows the control scheme employed for the proposed converter. The total number of switches are divided into two sets: first set S_{1a}, S_{1b}, S_{1c}, S_{1o} and second set S_{2a}, S_{2b}, S_{2c}, S_{2o}. The switches S_{1a}, S_{1b}, S_{1c} in first set are operated synchronously with same duty cycle d, and the switch S_{1o} is operated in complementary with a duty cycle $(1-d)$. The switches in second set are also operated in similar fashion i.e. the switches S_{2a}, S_{2b}, S_{2c} are operated synchronously with same duty cycle d, and the switch S_{2o} is operated in complementary with the duty cycle $(1-d)$. However, in each switching cycle, the gate signals to the second set of switches are phase-delayed by 180^0 with respect to the first set of switches. This phase-delayed operation between the two sets of switches i.e. between the two cells reduces the resultant input and output current ripple amplitudes substantially and doubles their effective ripple frequency which further reduces the input and output filter requirements for the interleaved converter.

B. Steady-State Analysis for One Switching Cycle

In the analysis, it is considered that the inductors values of the two cells are equal which makes both cells identical and symmetric. Therefore,

$$L_{1a,b,c} = L_{2a,b,c} = L \tag{1}$$

To simplify the understanding of converter operation, the converter input voltages and output voltage are considered constant in one switching cycle. The steady-state analysis is explained only for supply period $\omega t = 0$ to $\frac{\pi}{6}$ due to the symmetric nature of the converter. The same analysis can be extended and is valid for the remaining supply period as well. The inductors current waveforms of both the cells for converter duty cycles $d \leq 0.5$ and $d > 0.5$ are shown in Fig. 3 and Fig. 4, respectively. In both cases, it is observed that the two cells are working independently, and there are no circulating currents. As shown, the proposed converter exhibits total eight modes of operation in both the cases, and the input current ripple frequency is twice of the switching frequency. The relationship between the inductor's currents, and the currents before the filtering is given as

$$i_{(a,b,c)f} = i_{L1(a,b,c)} + i_{L2(a,b,c)} \tag{2}$$

Since the interleaved cells operation is independent and the individual cell steady-state operation is same as the single-cell converter reported in [32], the interleaved converter steady-state operation is not reported to evade the repetition.

III. Converter Design

A. DCM Condition

The converter duty cycle (d) limit to ensure the converter DCM operation from [32] is given as

$$d \leq \frac{M}{M+\sqrt{3}} \tag{3}$$

where $M = \frac{V_o}{V_m}$, is the converter voltage gain, V_o is the converter output voltage, and V_m is the supply peak voltage.

The converter critical voltage conversion ratio for the given duty cycle from (3) is given as

TABLE II
CONVERTER INPUT SPECIFICATIONS

Input line voltage	110 V ± 10%
Supply frequency, f_{in}	300-800 Hz
Rated power, P_o	2.0 kW
Output voltage, V_o	270 V
Switching frequency, f_s	50 kHz

$$M_{cr} \geq \frac{\sqrt{3}d}{1-d}. \quad (4)$$

B. Converter Average Output Current

From [32], each cell average output current is given as

$$i_{1o,avg} = i_{2o,avg} = \frac{9V_m^2 d^2 T_s}{4LV_o} \quad (5)$$

where T_s is switching time period.

The proposed interleaved converter is having two cells and connected in parallel at the DC output. Therefore, the converter average output current is equal to sum of the average output currents of the two cells and is given as

$$i_{o,avg} = \frac{9V_m^2 d^2 T_s}{2LV_o}. \quad (6)$$

C. Converter Input Current

Considering the converter operation is power loss free, then converter input power is equal to output power

$$\frac{3}{2}V_m I_m = V_o i_{o,avg} \quad (7)$$

$$I_m = \frac{3V_m d^2 T_s}{L} \quad (8)$$

where I_m is peak input current.

D. Inductor Design

The converter inductor design is explained with an example. The converter is designed for the input specifications mentioned in Table II. From input specifications, the converter gain M is

$$M = \frac{V_o}{V_{m,min}} = \frac{270}{80.82} = 3.341. \quad (9)$$

From (3), the converter maximum duty cycle limit is

$$d_{max} \leq \frac{3.341}{3.341+\sqrt{3}} \leq 0.6585. \quad (10)$$

From (6), the converter average output current for $d = 0.6585$, and $V_{m,min}$= 80.82 V is

$$i_{o,avg} = \frac{9.4412 \times 10^{-4}}{L}\ A. \quad (11)$$

From the input specifications, the converter output current is

$$I_o = \frac{P_o}{V_o} = \frac{2000}{270} = 7.4074\ A. \quad (12)$$

On equating (11) and (12), the converter inductor value to ensure the converter DCM operation up to the rated output power is found as 127.45 µH. In view of converter losses, the converter inductance value $L = 120$ µH is chosen for experimentation.

E. Output Capacitor Design

The output capacitor is designed based on the power holdup time required after the AC source disconnection. If t_h is the holdup time required to bring the output capacitor voltage to 90% of the rated voltage, then the output capacitance value required is given as

$$C_o = \frac{2P_o t_h}{(0.19V_o^2)}. \quad (13)$$

By considering a holdup time of 5 *mS*, the output capacitance calculated from (13) is C_o=1440 µF.

F. Input Filter Design

The two criteria for input filter design are

1. selection of cut-off frequency, f_c

$$f_c = \frac{1}{2\pi}\sqrt{\frac{3}{L_f C_f}} \quad (14)$$

2. minimization of filter reactive power consumption for the supply frequencies at rated output power. It is possible when the filter characteristic impedance is equal to the converter input impedance

$$Z_{ch} = Z_{in} \quad (15)$$

where Z_{ch} is characteristic impedance, and Z_{in} is converter input impedance at rated output power.

$$Z_{ch} = \sqrt{\frac{3L_f}{C_f}} \quad (16)$$

$$Z_{in} = \frac{L}{3d^2 T_s} \quad (17)$$

By using (14), and (16), the expressions for input low-pass filter parameters are given as

$$L_f = \frac{Z_{ch}}{2\pi f_c} \quad (18)$$

$$C_f = \frac{1}{6\pi f_c Z_{ch}}. \quad (19)$$

IV. COMPARISON OF PROPOSED INTERLEAVED CONVERTER WITH SINGLE-CELL CONVERTER

To establish the merits of the proposed interleaved converter, it is compared with the single-cell converter in terms of power density, efficiency and reliability for the same specifications and operating conditions. As a rule, the magnetic components (inductors or transformers), and the heat sinks occupy most of the converter volume and determine the power density, while the electrolytic capacitors determine the converter reliability. Then again, the heat sink size is directly determined by the total amount of semiconductor power losses incurred in the converter. Therefore, the analysis is carried out in terms of the semiconductor losses for estimating the heat sink size.

A. Inductors

In a converter, the inductors size basically depends on its inductance value and the amount of energy to be stored, which would be best described by the core area product (AP) formulae [33]. The AP formula described by (20) best suits for design of the filter inductors where the core loss is not severe, and the flux swing is limited by core saturation. The AP formula described

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TABLE III
ANALYTICAL COMPARISON OF THE INDUCTOR SIZES OF THE SINGLE-CELL AND THE PROPOSED INTERLEAVED CONVERTERS.

Description		Value (μH)	$i_{Lf,rms}$ or $i_{L,rms}$ (A)	i_{Lfsc} or Δi_L (A)	AP (cm^4)	Core	Core volume, V_e (cm^3)	Core weight (g)	Wire turns	wire size (mm^2)	Total weight (g)
DCM inductor	**Single-cell**	60	16.6	29.8	13.7	EE 5525	**104**	260	13	4.0	**310**
	Interleaved	120	8.16	14.9	5.33	EE 4220	**45.4**	112	22	2.5	**153**
Filter inductor	**Single-cell**	120	10.5	18.4	5.79	EE 4220	**45.4**	112	26	2.5	**162**
	Interleaved	40	10.5	18.4	1.33	EE 3512	**24.32**	62	16	2.5	**92**

by (21) best suits for design of the DCM operated inductors where the flux swing is limited by its core loss.

$$AP = A_e A_w = \left(\frac{10^4 L_f i_{Lfsc} i_{Lf,rms}}{B_m J_m K_p}\right)^{4/3} \text{ cm}^4 \quad (20)$$

$$AP = A_e A_w = \left(\frac{10^4 L\, \Delta i_L\, i_{L,rms}}{\Delta B_m J_m K_p}\right)^{4/3} \text{ cm}^4 \quad (21)$$

where

L_f = filter inductance value, H

i_{Lfsc} = maximum short circuit peak current through filter inductance, A

$i_{Lf,rms}$ = filter inductance maximum RMS current, A

B_m = core saturation flux density, T

L = DCM inductance value, H

Δi_L = maximum current swing, A

ΔB_m = maximum flux density swing, T

$i_{L,rms}$ = DCM inductance maximum RMS current, A

J_m = maximum current density; 450 A/cm^2 for filter inductor, 297 A/cm^2 for DCM inductor

K_p = 0.4, window area utilization factor.

Table III compares the single-cell and interleaved converters inductances values, RMS, peak currents through them, the calculated area product, the selected core volume, and its calculated weight. The filter inductance values for both converters are selected with a consideration of the same input current ripple attenuation after filtering. The core material is chosen based on minimizing the core loss where the ferrite core EE-3C92 type material has been selected because of its low core loss and high saturation flux density. The inductors maximum rms and peak currents are calculated at rated output power from the formulae (22) to (25).

$$i_{L,rms} = \frac{V_m d T_s}{L}\sqrt{\frac{V_m d}{2\pi V_o}\left(\frac{\pi V_o}{V_m} + 4(3-\sqrt{3})\right)} \quad (22)$$

$$\Delta i_L = \frac{\sqrt{3} V_m d T_s}{L} \quad (23)$$

$$i_{Lf,rms} = \frac{3 V_m d^2 T_s}{2\sqrt{2} L} \quad (24)$$

$$i_{Lfsc} = \frac{V_m}{Z_{in}} \quad (25)$$

From Table III, it is observed that the volume and weight of the DCM inductor in interleaved converter is reduced by more than half when compared to the single-cell converter. To prove the analytical calculations and to get the actual physical interpretation, the DCM inductors have been prepared at lab with the cores specified in Table III and are shown in Fig. 5

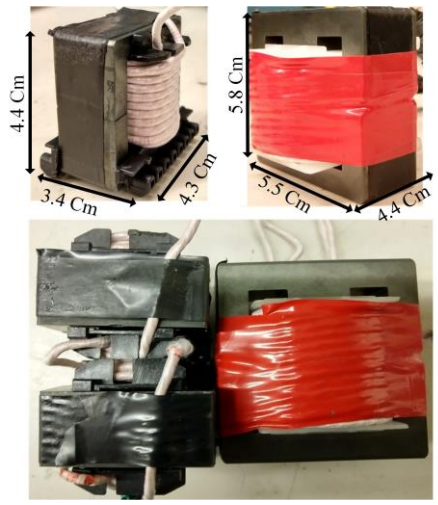

Fig. 5. The pictures of the DCM inductors prepared in lab; left side is the interleaved inductor; right side is the single-cell inductor.

along with their dimensions. The left side is the interleaved DCM inductor with volume 64.32 cm^3, weight 165 g, and the right side is the single-cell DCM inductor with volume 140.36 cm^3, weight 350 g. It confirms that the actual measures are in-line with the analytically estimated values. It is also observed that two DCM inductors of interleaved converter have occupied the same space as one DCM inductor of single-cell converter as depicted in Fig. 5. Since the interleaved converter employs the DCM inductors as twice of the single-cell topology, the 50% reduction in volume and weight compensates the extra DCM inductors count in interleaved converter. Therefore, the interleaved converter would not occupy more volume compared to the single-cell converter for the count of DCM inductors.

In case of filter inductor, both converters employ the same number of filter inductors. Since the filter inductor size and weight is almost half in interleaved converter when compared to the single-cell converter which clearly evidences the higher power density and the higher power to weight ratio of the interleaved converter. For higher power requirements, either the number of interleaved cells can be increased, or the individual cell power levels can be increased. In both the scenarios, the filter and DCM inductor power losses will increase in proportional to the converter power.

B. Semiconductor Power Losses

Table IV lists the semiconductors loss breakdown of both the converters for rated output power. In calculation, it is assumed that both the converters employed the same switches (UJ3C065030K3S, SIC, 650V, 30 *m*ohm), and the diodes

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TABLE IV

THE SEMICONDUCTORS LOSSES BREAKDOWN FOR THE SINGLE-CELL CONVERTER, AND THE INTERLEAVED CONVERTER AT 2.0 KW OUTPUT POWER.

Description	Single-cell	Interleaved	
Input switch rms current	16.41	8.20	A
Input switch turn-off average current	34.30	17.15	A
Output switch rms current	-----	7.80	A
Output switch turn-on average current	-----	25.73	A
Bridge diode rms current	8.286	4.19	A
Bridge diode average current	2.47	1.254	A
Switches switching losses	9.16	9.16	W
Switches conduction losses	24.23	15.75	W
Bridge diode conduction losses	13.71	12.24	W
Total semiconductor losses	47.10	37.15	W

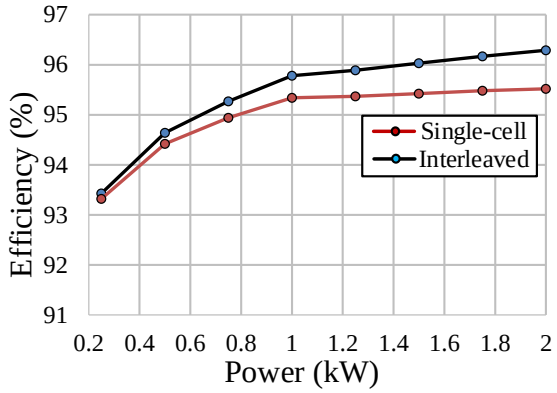

Fig. 6. The calculated efficiency curves of single-cell and interleaved converters.

(RHRG5060-F085, 600 V) for the operation. The semiconductors losses have been calculated from the loss formulae described in [33]. From Table IV, it is observed that the total semiconductors losses in case of interleaved converter are less by 10 W when compared to the single-cell converter. If the same type of cooling mechanism and the same material is used for the heat sink design, then the heat sink size requirement in case of interleaved converter is reduced by 26.78 % in order to maintain the same junction temperature for the semiconductor devices. Therefore, the reduction in heat sink size clearly enhances the interleaved converter power density and reduces the converter total weight. Fig. 6 depicts the calculated efficiency curves of both the converters for different output powers. It clearly demonstrates the efficiency of the interleaved converter is high when compared to the single-cell converter which is due to the reduction in semiconductor losses as well as filter losses.

C. Capacitors

In a converter, the electrolytic capacitors are the most fragile components and decides the lifespan or reliability of the system. By considering the operating temperatures of both the converters same, then the expected life of a capacitor with respect to the ripple current passing through at the given operating condition [35], [36] is given as

$$Life_{exp} = Life_{base} * 2^{\left(K_t i_{a,ripple}^2 R_{ESR}\left(1-\left(\frac{i_{a,ripple}}{i_{r,ripple}}\right)^2\right)\right)} \quad (26)$$

TABLE V

NUMERICAL VALUES OF CAPACITORS RIPPLE CURRENTS IN SINGLE-CELL AND INTERLEAVED CONVERTERS.

Description		Value (μF)	Maximum ripple current (A)	Ripple frequency (kHz)
Output filter capacitor	**Single-cell**	1440	51.4	50
	Interleaved	1440	25.8	100
Input filter capacitor	**Single-cell**	1.1	30.16	50
	Interleaved	0.4	14.7	100

TABLE VI

HARDWARE SETUP SPECIFICATIONS

Component	Specifications
Switches	UJ3C065030K3S, SIC, 650V, 30 *m*ohm
Diodes	RHRG5060-F085, 600 V
Output capacitor, C_o	ESMQ401VSN471MQ50W, 3 x 470 μF
Filter capacitors, C_f	F873DU104M760Z, 4 x 0.1 μF
Filter inductors, L_f	1140-820K-RC, 82/2 μH
Snubber capacitor	R75QD0470DQ30J, 470 pF
Snubber resistor	EP5WS100RJ, 100 Ω
Inductors, $L_{1r,y,b}, L_{2r,y,b}$	42 x 21 x 20, EE Ferrite cores
Gate drivers	HCNW3120 IC
Power source	California-MX30 (300 – 500 Hz)

where

$Life_{base}$: Capacitor life specified in datasheets at the rated operating condition

$i_{a,ripple}$: Actual ripple current through the capacitor

$i_{r,ripple}$: Rated ripple current of the capacitor

R_{ESR}: Equivalent series resistance of the capacitor

K_t: $55/S^{0.8}$, 'S' is capacitor surface area in cm^2.

From (26), it is clear that when the actual ripple current through the capacitor is approaching the rated ripple current, the factor $\left(1-\left(\frac{i_{a,ripple}}{i_{r,ripple}}\right)^2\right)$ is moving towards zero, and the expected life of capacitor is getting reduced and approaching the '$Life_{base}$'. That means, if the ripple current through the capacitor is minimized, then the lifespan of the capacitor will be enhanced, and thereby it increases the converter reliability.

Table V lists the numerical values of capacitors ripple currents for both single-cell, and interleaved converters at rated output power. The capacitors ripple current with interleaved operation is reduced by 50 % and its effective frequency is doubled. This 50 % ripple current reduction in interleaved converter helped in enhancing the lifespan of output electrolytic capacitors by 2.71 times when compared to the single-cell converter. The calculation is done using (26) with a consideration of both converters employed the same filter capacitors (ESMQ401VSN471MQ50W), and the single-cell output filter capacitors are operating at rated ripple current. Further, the increase in effective ripple frequency of the interleaved converter increases the ripple current handling capability of the capacitors, which further helps in enhancing the capacitors lifespan and the system reliability.

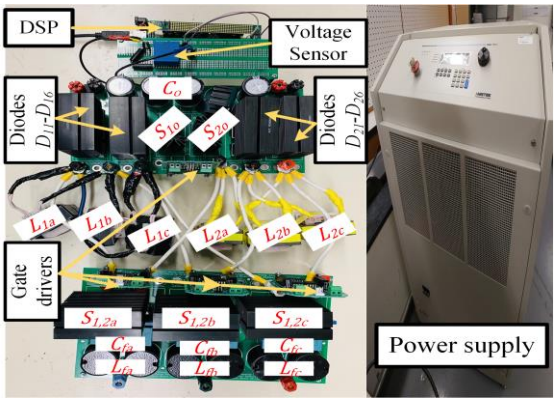

Fig. 7. A 2.0 kW hardware prototype of proposed converter.

TABLE VII

CONVERTER INPUT PF AND CURRENT THD (%) FOR DIFFERENT OUTPUT POWERS FOR SUPPLY FREQUENCIES 300 HZ AND 500 HZ.

Power (kW)	300 Hz		500 Hz	
	PF	THD (%)	PF	THD (%)
0.25	0.9969	5.39	0.9956	5.35
0.5	0.9983	5.20	0.9978	5.19
0.75	0.9990	4.20	0.9989	4.19
1.0	0.9994	3.33	0.9994	3.33
1.5	0.9995	3.05	0.9995	3.04
2.0	0.9996	2.70	0.9996	2.52

TABLE VIII

COMPARISON OF THE PROPOSED INTERLEAVED CONVERTER WITH STATE-OF-THE-ART INTERLEAVED BOOST CONVERTERS

Description	Conduction mode of operation	Control	Number of semiconductors			Number of passive components			Filter requirement for the same power quality	Reported efficiency and power
			Switches	Diodes	Total	Inductors	Capacitors	Total		
Three-phase interleaved single-switch boost rectifier [28]	DCM	Simple	4	18	22	11	6	17	High	94.0 % at 8.0 kW
Three-phase interleaved semi-controlled boost rectifier [38]	DCM	Simple	6	8	14	9	4	13	High	97.0 % at 4.0 kW
Three-phase six-switch interleaved Vienna rectifier [39]	CCM	Complex	12	14	26	6	2	8	Low	97.5 % at 10.0 kW
Three-phase interleaved single-stage PFC rectifier [40]	CCM	Complex	4	16	20	9	3	12	Low	92.5 % at 1.1 kW
Three-phase interleaved single-stage PFC rectifier with flying capacitor [41]	CCM	Complex	4	16	20	9	4	13	Low	93.0 % at 1.1 kW
Three-phase interleaved PWM single-stage resonant rectifier [42]	CCM	Complex	12	6	18	9	5	14	Low	96.3 % at 2.0 kW
Proposed Converter	DCM	Simple	8	12	20	9	4	13	Low	96.3 % at 2.0 kW

V. EXPERIMENTAL RESULTS

To demonstrate the proposed converter UPF operation and the control scheme for MEA variable supply frequencies, a 2.0 kW concept-proof laboratory prototype (not optimized for efficiency and power density) has been built with the designed parameters and is depicted in Fig. 7. The components specifications employed to develop the hardware prototype are listed in Table VI. The converter control-to-output voltage transfer function has been obtained using average current injected equivalent circuit approach [32], [37] and is given in (27). A PI controller $\left(k_p + \frac{k_i}{s}\right)$ with gains $k_p = 0.03$ and $k_i = 6.3$ is designed for the converter closed-loop operation for the control design specifications of gain cross over frequency 100 Hz, and phase margin 75^0. The designed controller is programmed in the digital control platform DSP TMS320F28335 and the hall-effect sensor LEM LV-25P has been employed to sense the converter output voltage.

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{1062}{0.0525\,S + 2.278} \qquad (27)$$

Fig. 8(a) and Fig. 8(b) depict the measured input currents and output voltage at rated output power for supply frequency 300 Hz and 500 Hz, respectively. The input currents are sinusoidal and balanced, and the output voltage is stable and constant at reference value 270 V. Fig. 8(c) and Fig. 8(d) depict the measured converter input voltage and input currents of one phase at rated output power for supply frequency 300 Hz and 500 Hz, respectively. The input current is very closely following the input voltage both in phase and shape and confirming the converter UPF operation. Fig. 8(e) and Fig. 8(f) depict the input current harmonic spectrum at rated output power for supply frequency 300 Hz and 500 Hz, respectively. The measured input current THD is less than 3 % in both cases and the input power factor is very close to unity. The converter measured input power factor and the input current THD (%) for different output powers for supply frequency 300 Hz and 500 Hz are listed in Table VII. The converter minimum input power factor is 0.9956 (almost unity) and the maximum input current THD is 5.39 %. Fig. 8(g) depicts the converter response for supply frequency change from 300 Hz to 500 Hz. The output voltage is stable and steady at 270 V, and no oscillations are observed during the supply frequency change. The input current is closely tracking the input voltage during the supply frequency change as well. Fig. 8(h) depicts the inductors current waveforms of one interleaved cell at rated output power. The inductors currents are discontinuous and confirming the converter design. Fig. 8(i) depicts the measured unfiltered input currents of the proposed converter at rated output power where the maximum current ripple of 30.4 A is measured which is near to $\sqrt{3}$ times (due to Δ

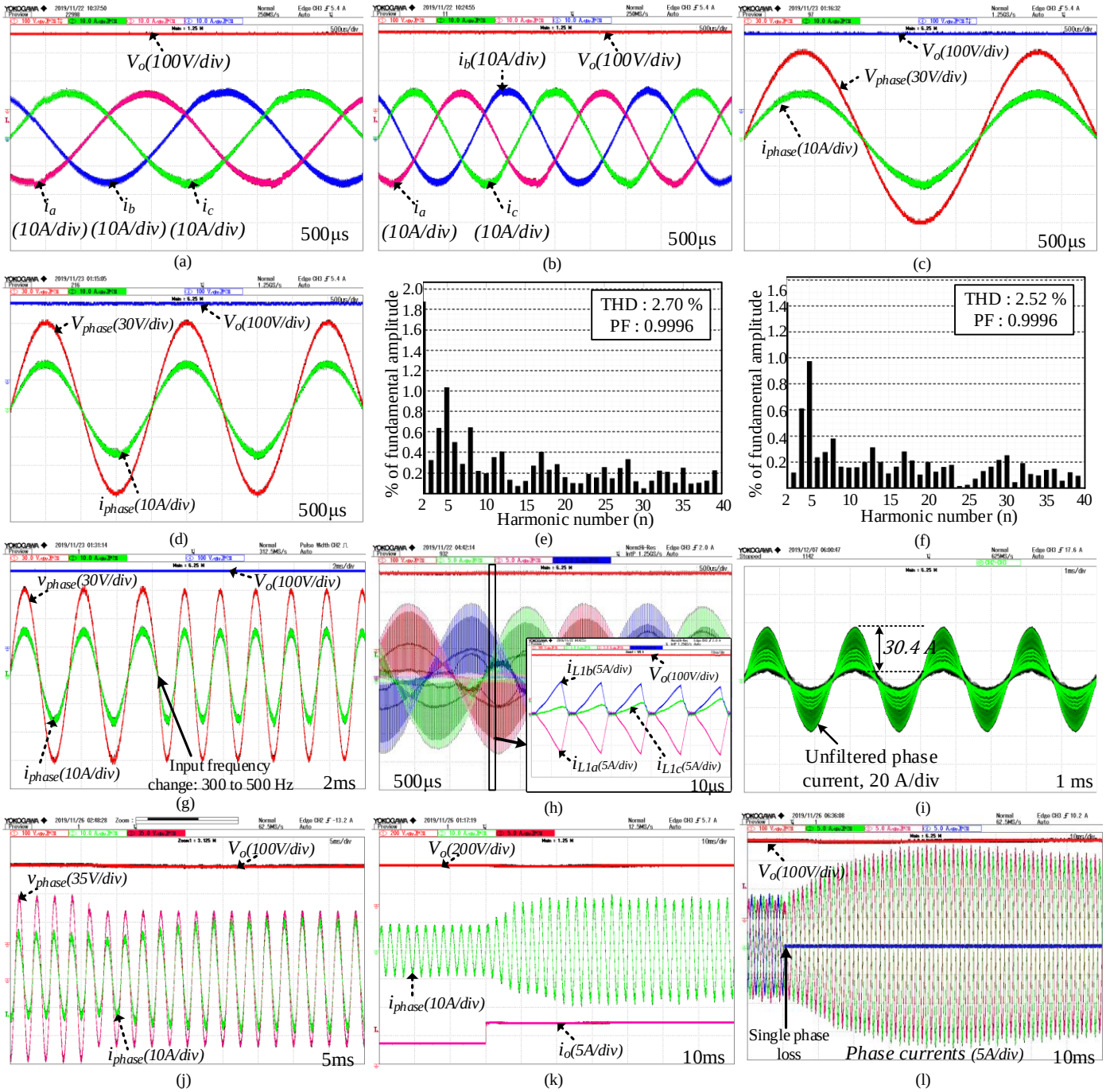

Fig. 8. Experimental results at rated output power (a), (b) input currents and output voltage for supply frequency 300 Hz and 500 Hz; (c), (d) input voltage and input current of one phase for supply frequency 300 Hz and 500 Hz; (e), (f) input current harmonic spectrum for supply frequency 300 Hz and 500 Hz; (g) converter response for supply frequency change from 300 to 500 Hz; (h) inductor currents of one cell; (i) unfiltered input currents; (j) converter response for 20 % input voltage perturbation; (k) converter response for 50 % load perturbation from 1.0 kW to 2.0 kW; (l) converter response for a single-phase loss.

connection) of the input filter capacitor current ripple mentioned in Table V, and thus validating the analytical results. Fig. 8(j) depicts the converter response for 20 % input voltage decremental perturbation at rated output power where the converter input current is increased in the same proportion as reduction in input voltage to maintain the power balance between input and output. Fig. 8(k) depicts the converter response for 50 % load incremental perturbation from 1.0 kW to 2.0 kW. The converter response is instantaneous, and the output voltage is closely tracking the reference voltage 270 V, thus validating the robustness of the designed controller. Further, the proposed converter provides the fault tolerant operation for single-phase loss and provides half of the rated output power without altering the controller structure which is one of the desired features to be met for MEA application. The reduction in deliverable power is due to the duty cycle limit defined in (3). With single-phase loss, the converter resembles a single-phase converter with line-to-line voltage as input source. Therefore, the output voltage has second order supply frequency

oscillations like a single-phase PFC converter, as depicted in Fig. 8(l).

Table VIII illustrates the comparison of the proposed converter with the state-of-the-art interleaved boost converters. The comparison criteria include the conduction mode of operation, control complexity, total number of semiconductors, total number of passive components, current harmonic distortion, and efficiency. It can be observed that the DCM operation simplifies the control, and the filter requirement is low for the same power quality in the proposed interleaved buck-boost derived converter which is due to the absence of lower order harmonics in the input current unlike the DCM interleaved boost converters present lower order 5^{th} and 7^{th} harmonics. The efficiency of the proposed converter is 96.3% which is comparable to the efficiency of state-of-the-art interleaved boost converters.

VI. Conclusion

In this paper, a three-phase interleaved buck-boost-derived PFC converter for MEA is proposed, analyzed, and designed. For the wide supply frequency variation of MEA, the converter UPF operation at all supply frequencies has been achieved through the inherent PFC characteristic of DCM by employing only single sensor. The converter output voltage is regulated with a simple voltage control loop. An analytical comparison of the proposed interleaved converter with single-cell converter in terms of power density, efficiency and reliability has been made and the relevant results has been presented. The filter, and the DCM inductors size and weight in interleaved converter is reduced by half when compared to the single-cell converter. The heat sink requirement is less by 26.78 % in interleaved converter which shows the higher power density, and the higher power to weight ratio of the proposed interleaved converter. The reduction in filter and semiconductor losses depicted high efficiency for the interleaved converter. The interleaved operation enhanced the lifespan of filter capacitors by more than two times which is due to the reduction of current ripples through the capacitors. However, the initial cost of the interleaved converter is high since greater number of components are required for its operation. A 2.0 kW laboratory hardware prototype has been built as a proof-of-concept experimentation. It is shown that the converter is maintained UPF operation for all powers and for all supply frequencies. A high input power factor of 0.9996 and a minimum current THD of 2.52 % are recorded from the developed laboratory prototype.

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